FIG. 1A

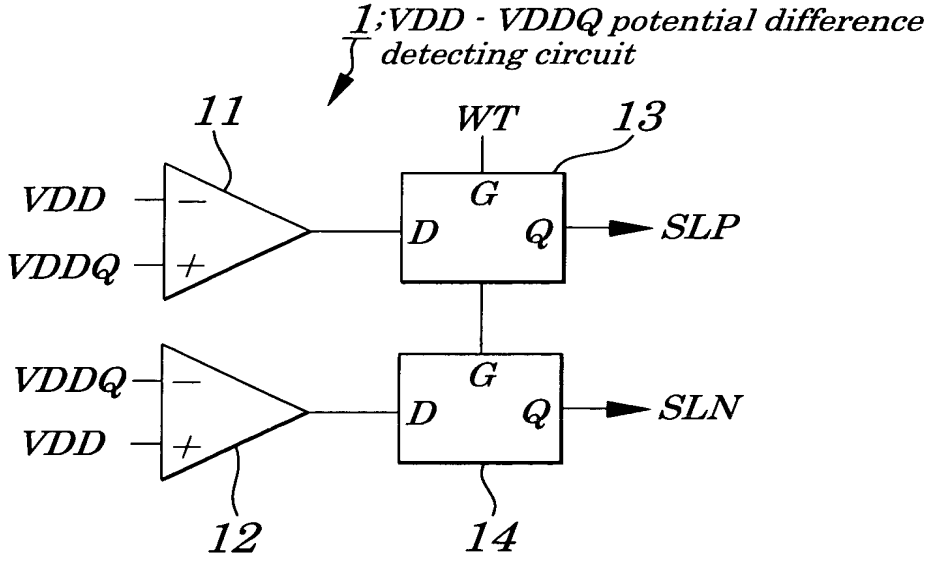

1;VDD - VDDQ potential difference detecting circuit
11
WT
13
VDD
VDDQ
G
D
Q
SLP
VDDQ
VDD
G
D
Q
SLN
12
14

FIG. 1B

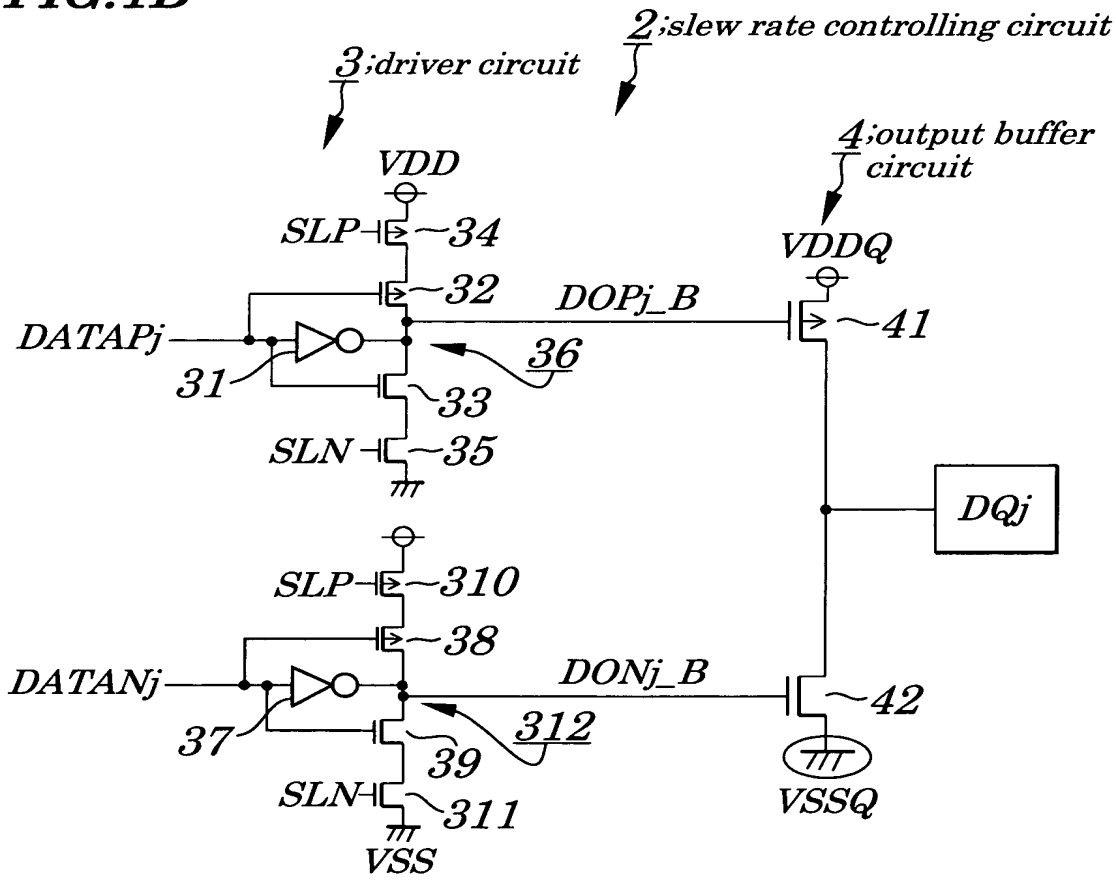

2;slew rate controlling circuit
3;driver circuit
4;output buffer circuit
VDD
SLP
34
32
DOPj_B
DATAPj
31
36
33
SLN
35
VDDQ
41
DQj
SLP
310
38
DONj_B
DATANj
37
312
39
42
SLN
311
VSS
VSSQ

FIG.2

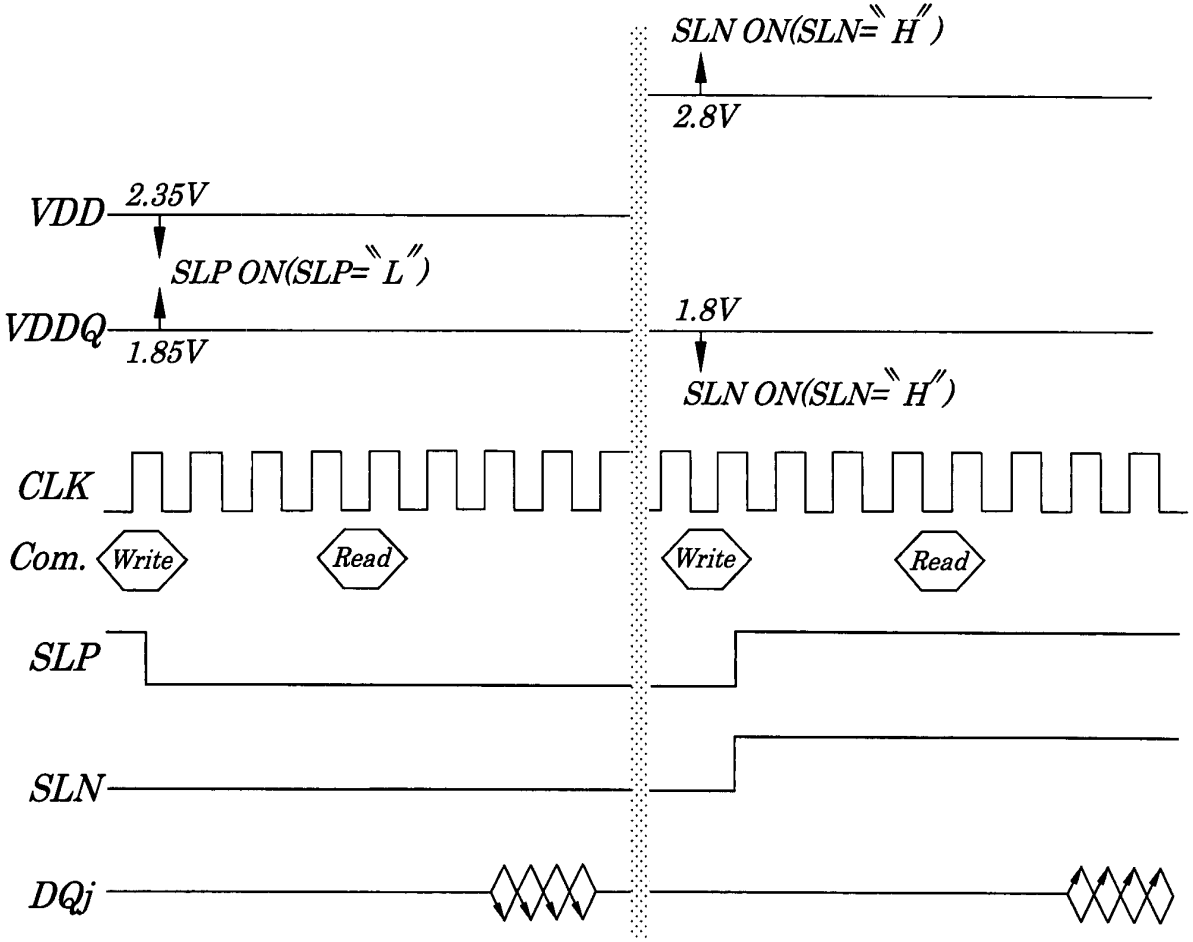

SLN ON(SLN="H")
2.8V
VDD
2.35V
SLP ON(SLP="L")
VDDQ
1.85V
1.8V
SLN ON(SLN="H")
CLK
Com.
Write
Read
Write
Read
SLP
SLN
DQj

FIG.3

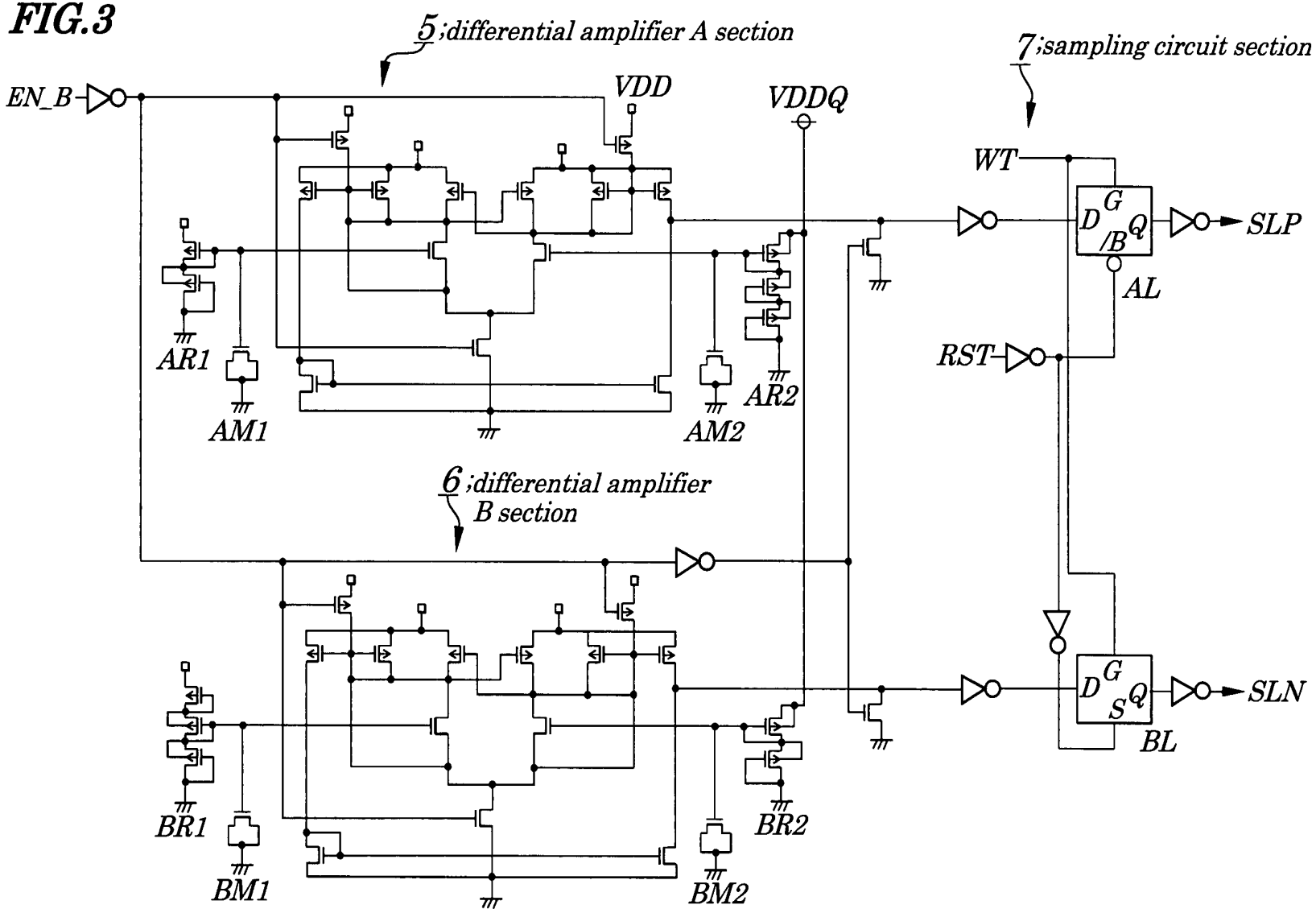

5;differential amplifier A section
7;sampling circuit section
EN_B
VDD
VDDQ
WT
SLP
AL
AR1
AM1
AM2
AR2
RST
6;differential amplifier B section
SLN
BL
BR1
BM1
BM2
BR2

FIG.4

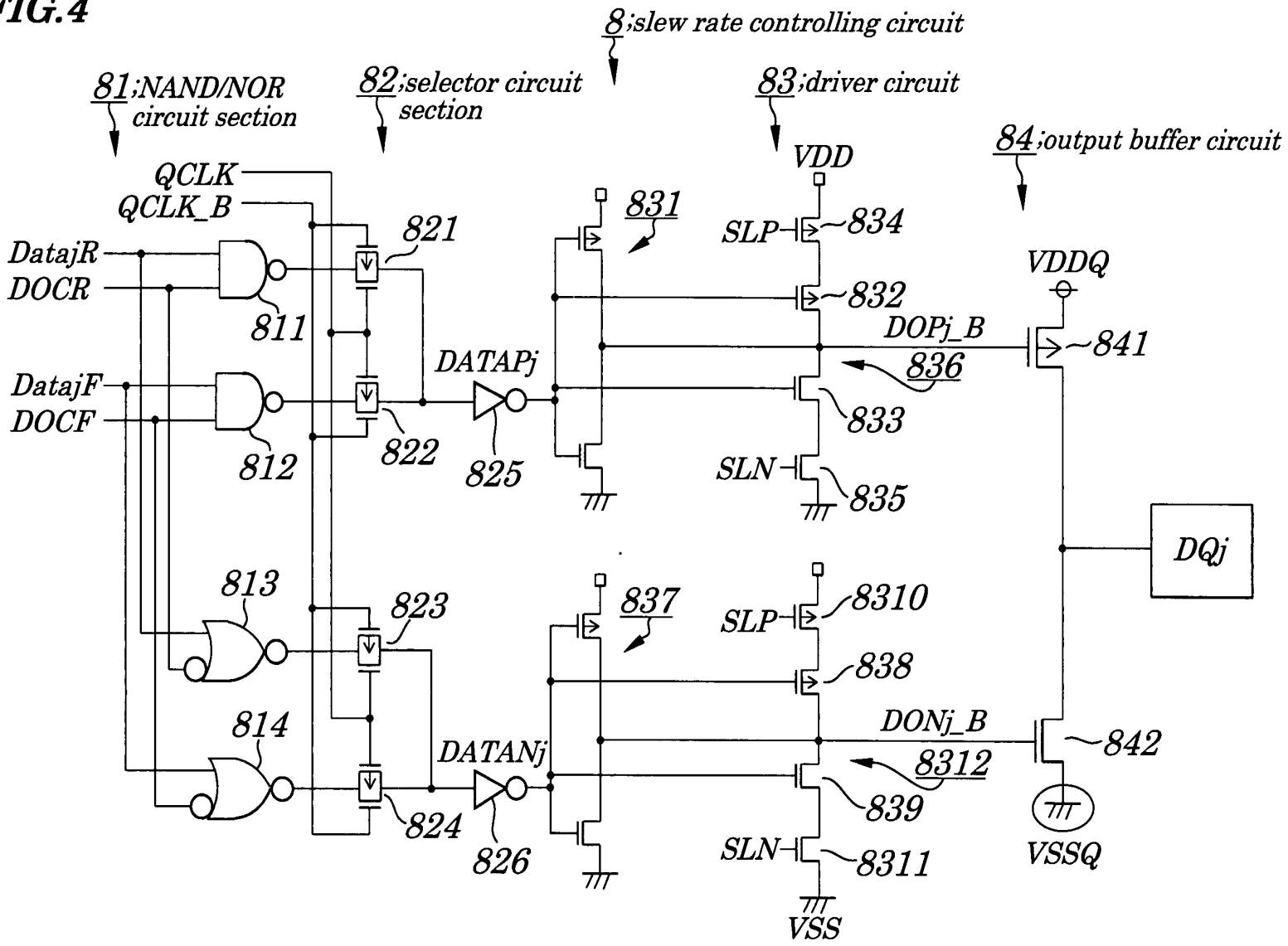

8;slew rate controlling circuit
81;NAND/NOR circuit section
82;selector circuit section
83;driver circuit
84;output buffer circuit
QCLK
QCLK_B
DatajR
DOCR
DatajF
DOCF
811
812
813
814
821
822
823
824
825
826
DATAPj
DATANj
831
837
VDD
SLP
834
832
833
SLN
835
DOPj_B
836
VDDQ
841
DQj
8310
838
DONj_B
842
8312
839
8311
VSSQ
VSS

FIG.5

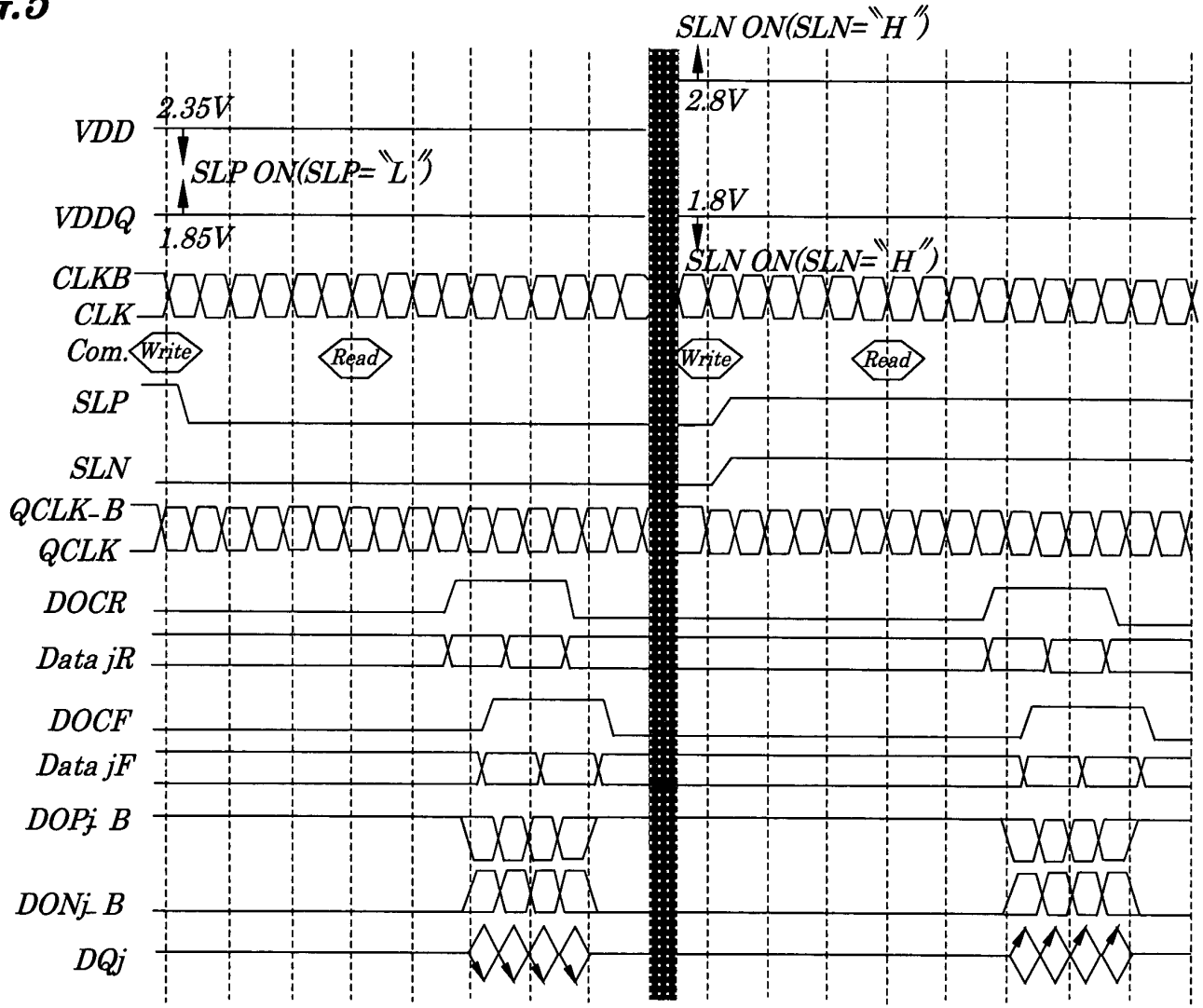

SLN ON(SLN="H")
2.35V
VDD
SLP ON(SLP="L")
VDDQ
1.85V
2.8V
1.8V
SLN ON(SLN="H")
CLKB
CLK
Com.
Write
Read
Write
Read
SLP
SLN
QCLK-B
QCLK
DOCR
Data jR
DOCF
Data jF
DOPj B
DONj B
DQj

FIG.6

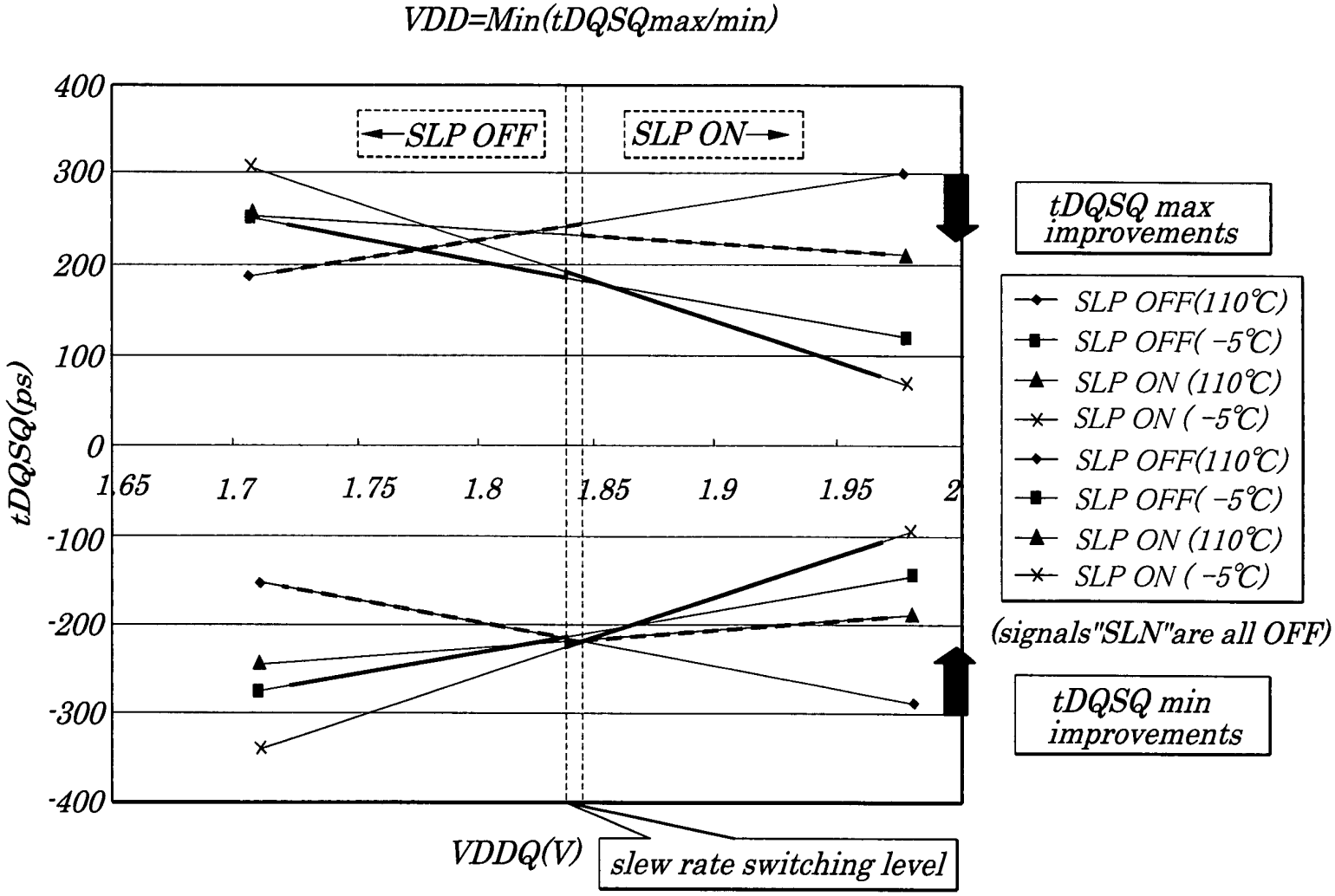
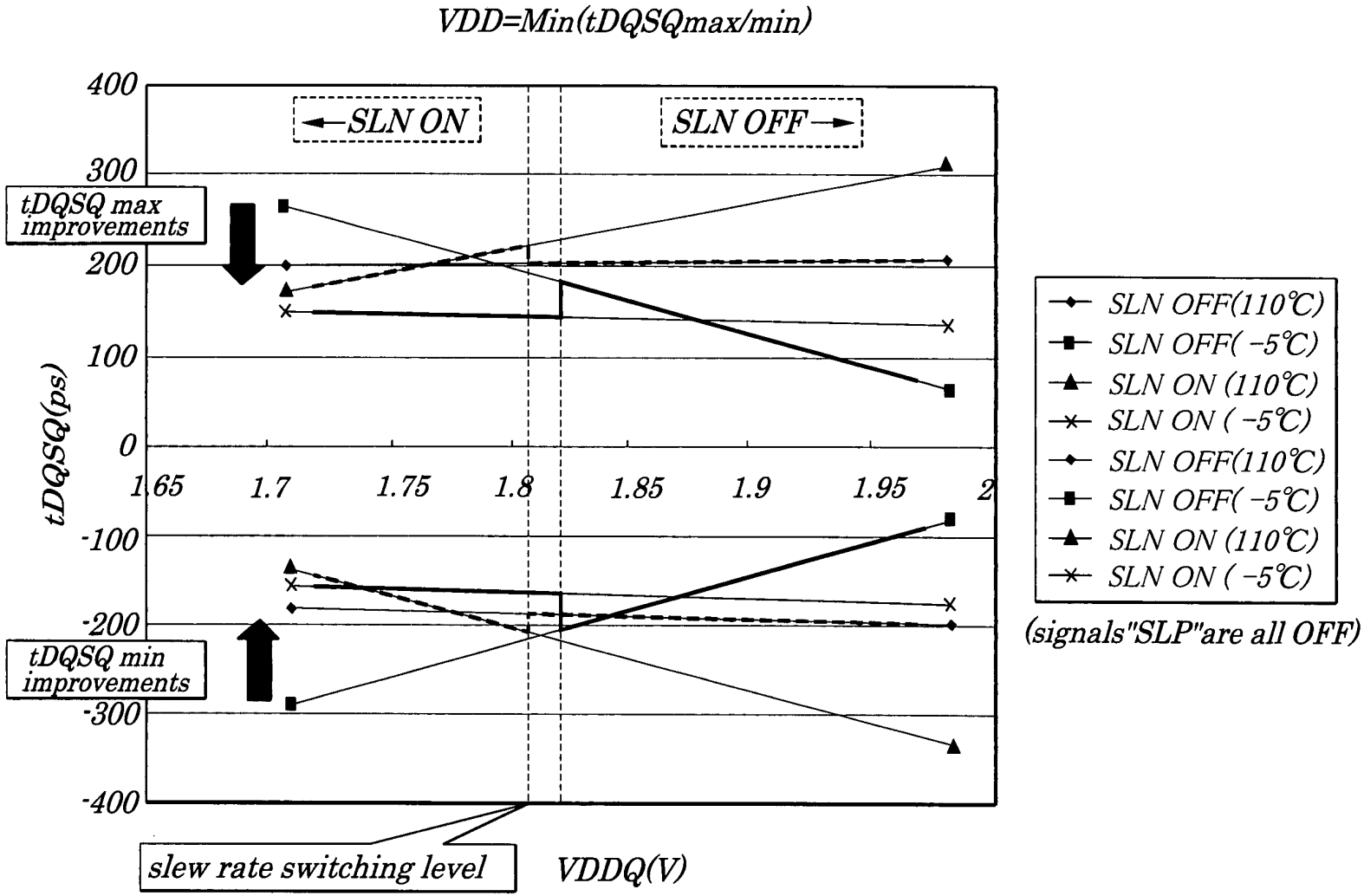

VDD=Min(tDQSQmax/min)
400
300
200
100
0
-100
-200
-300
-400
tDQSQ(ps)
1.65
1.7
1.75
1.8
1.85
1.9
1.95
2
SLP OFF
SLP ON
VDDQ(V)
slew rate switching level
tDQSQ max improvements
SLP OFF(110℃)
SLP OFF(-5℃)
SLP ON (110℃)
SLP ON (-5℃)
SLP OFF(110℃)
SLP OFF(-5℃)
SLP ON (110℃)
SLP ON (-5℃)
(signals"SLN"are all OFF)
tDQSQ min improvements

FIG. 7


VDD=Min(tDQSQmax/min)
400
300
200
100
0
-100
-200
-300
-400
tDQSQ(ps)
←SLN ON
SLN OFF→
tDQSQ max improvements
tDQSQ min improvements
1.65
1.7
1.75
1.8
1.85
1.9
1.95
2
slew rate switching level
VDDQ(V)
SLN OFF(110℃)
SLN OFF(-5℃)
SLN ON (110℃)
SLN ON (-5℃)
SLN OFF(110℃)
SLN OFF(-5℃)
SLN ON (110℃)
SLN ON (-5℃)
(signals"SLP"are all OFF)